



PMZB950UPE

20 V, P-channel Trench MOSFET

28 July 2014

Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1006B-3 (SOT883B) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Trench MOSFET technology
- Leadless ultra small and ultra thin SMD plastic package: $1.0 \times 0.6 \times 0.37$ mm
- ElectroStatic Discharge (ESD) protection > 1 kV HBM
- Drain-source on-state resistance $R_{DSon} = 1.02 \Omega$

3. Applications

- Relay driver
- High-speed line driver
- High-side load switch
- Switching circuits

4. Quick reference data

Table 1. Quick reference data

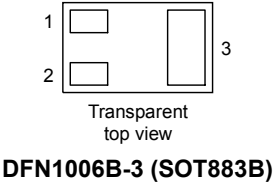
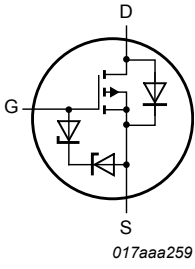
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25 \text{ }^\circ\text{C}$	-	-	-20	V
V_{GS}	gate-source voltage		-8	-	8	V
I_D	drain current	$V_{GS} = -4.5 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$	[1]	-	-500	mA
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5 \text{ V}; I_D = -500 \text{ mA}; T_j = 25 \text{ }^\circ\text{C}$	-	1.02	1.4	Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm^2 .



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>Transparent top view DFN1006B-3 (SOT883B)</p>	 <p>017aaa259</p>
2	S	source		
3	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMZB950UPE	DFN1006B-3	DFN1006B-3: leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.37 mm	SOT883B

7. Marking

Table 4. Marking codes

Type number	Marking code
PMZB950UPE	0101 1001

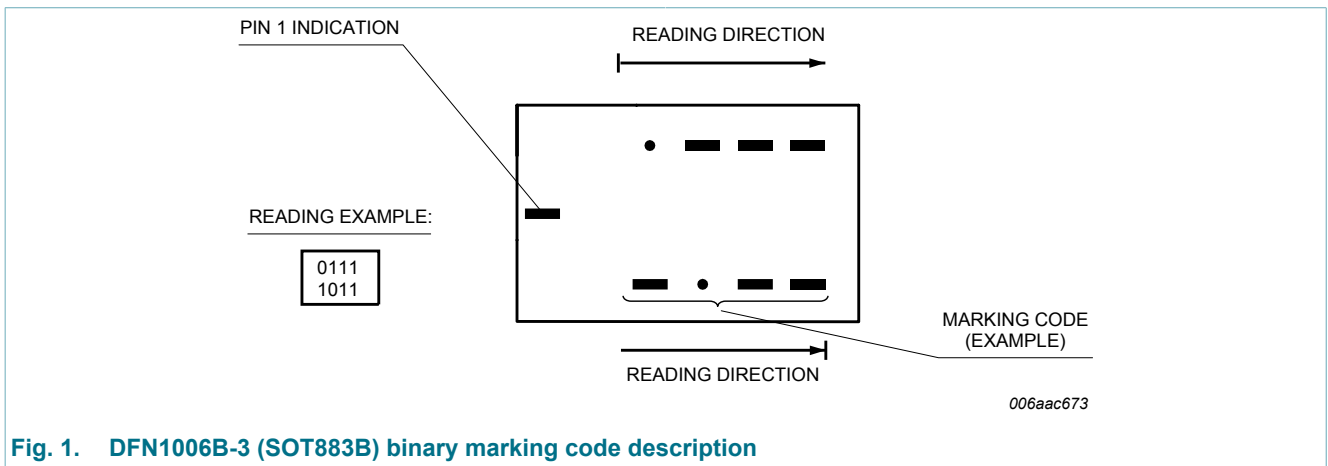


Fig. 1. DFN1006B-3 (SOT883B) binary marking code description

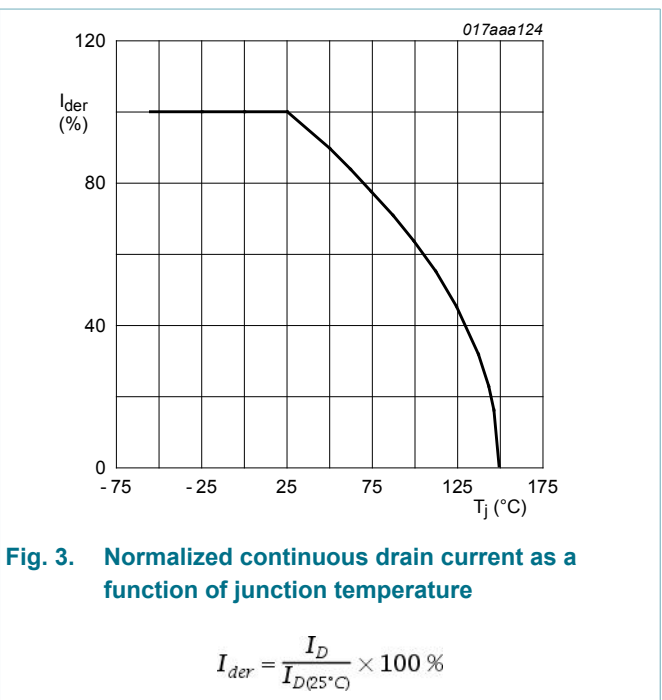
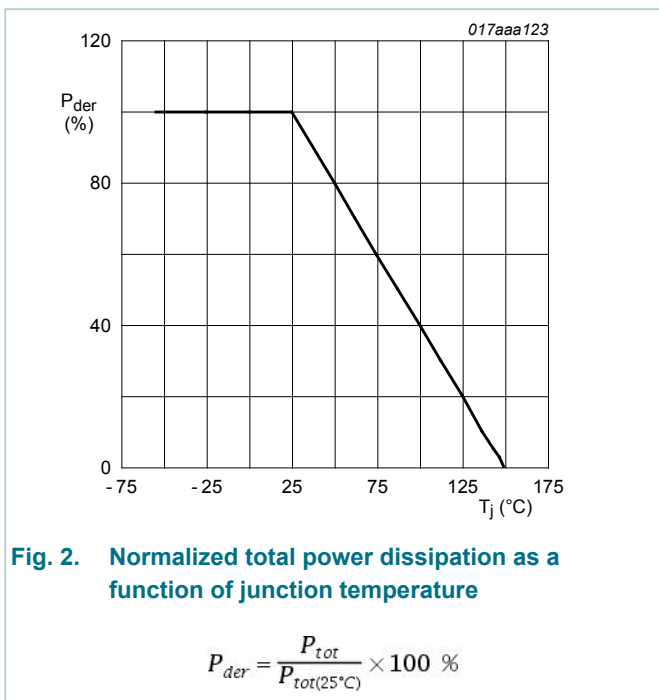
8. Limiting values

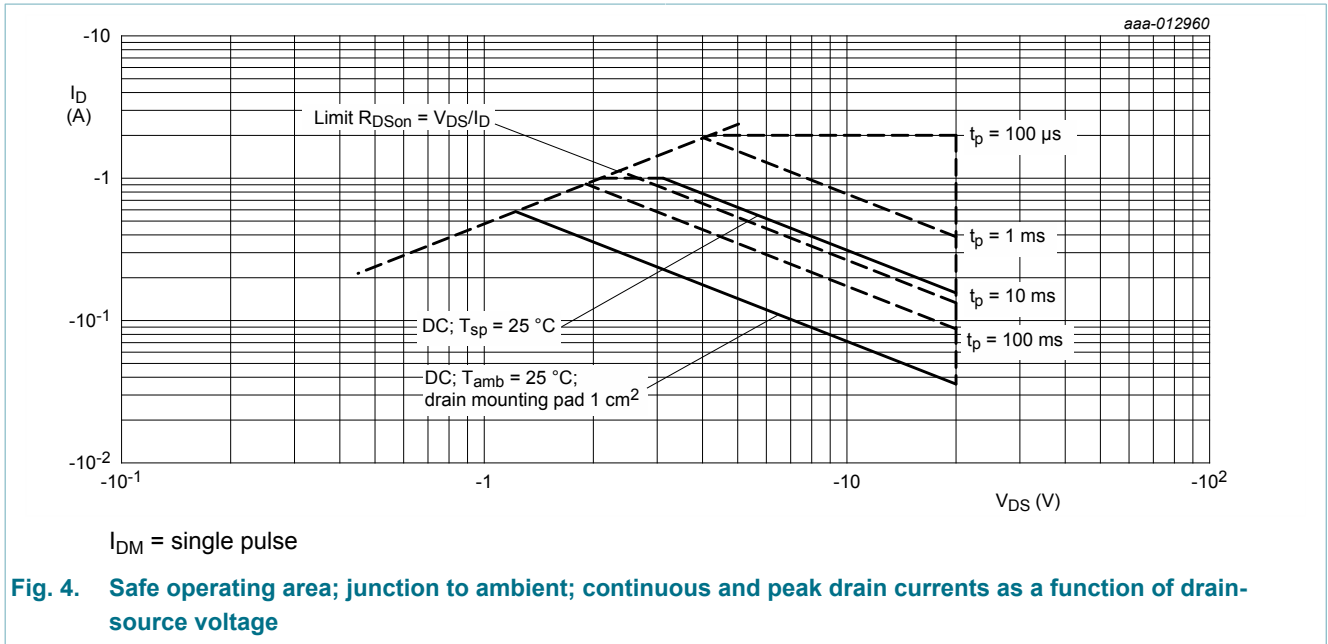
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-20	V
V _{GS}	gate-source voltage			-8	8	V
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C	[1]	-	-500	mA
		V _{GS} = -4.5 V; T _{amb} = 100 °C	[1]	-	-300	mA
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	-2	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	360	mW
			[1]	-	715	mW
		T _{sp} = 25 °C		-	2700	mW
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	-350	mA

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm².
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.





9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	305	360	K/W
			[2]	-	150	175	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	40	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm^2 .

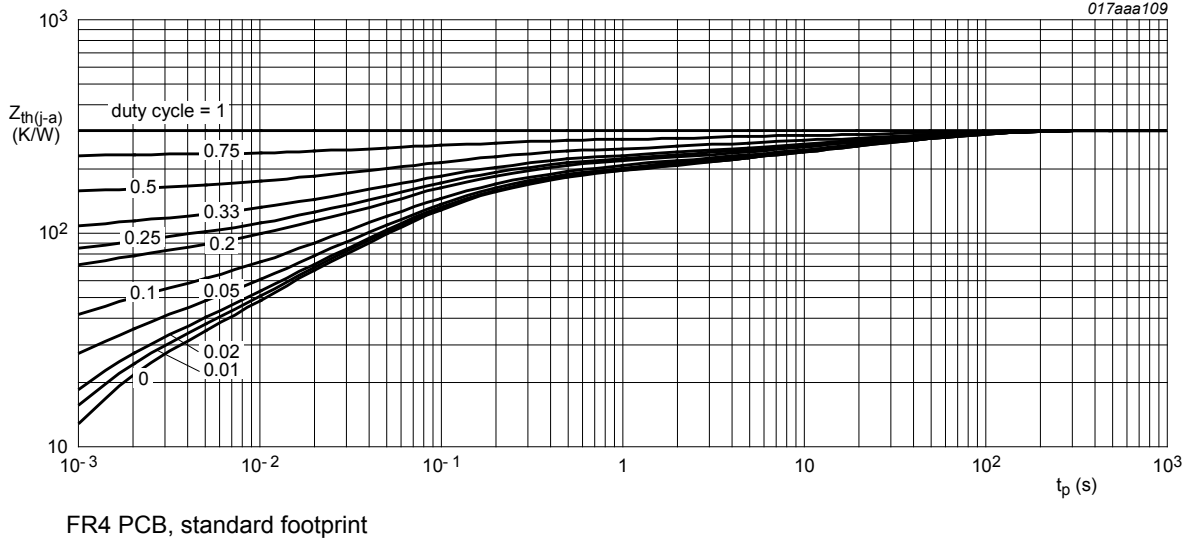


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

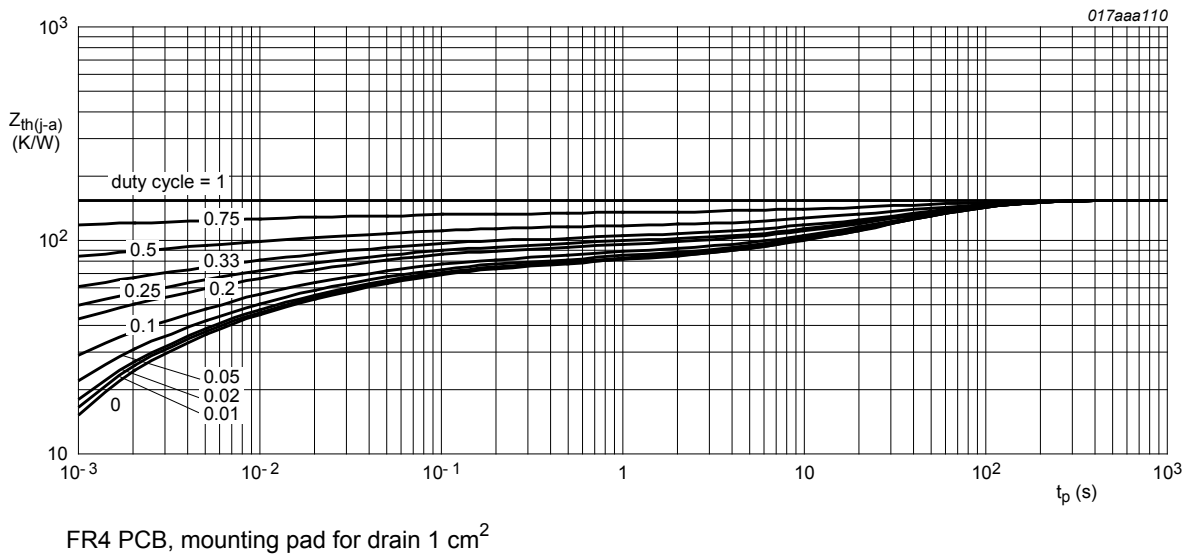


Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-20	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	-0.45	-0.7	-0.95	V
I_{DSS}	drain leakage current	$V_{DS} = -20 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-1	μA
		$V_{DS} = -20 V; V_{GS} = 0 V; T_j = 150 \text{ }^\circ C$	-	-	-10	μA
I_{GSS}	gate leakage current	$V_{GS} = 8 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	10	μA
		$V_{GS} = -8 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-10	μA
		$V_{GS} = -4.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-1	μA
		$V_{GS} = 4.5 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	1	μA
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5 V; I_D = -500 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	1.02	1.4	Ω
		$V_{GS} = -4.5 V; I_D = -500 \text{ mA}; T_j = 150 \text{ }^\circ C$	-	1.54	2.1	Ω
		$V_{GS} = -2.5 V; I_D = -200 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	1.27	2.2	Ω
		$V_{GS} = -1.8 V; I_D = -40 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	1.7	3.3	Ω
		$V_{GS} = -1.5 V; I_D = -10 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	2.3	5	Ω
		$V_{GS} = -1.2 V; I_D = -1 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	3.5	-	Ω
g_{fs}	forward transconductance	$V_{DS} = -10 V; I_D = -500 \text{ mA}; T_j = 25 \text{ }^\circ C$	-	480	-	mS
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -10 V; I_D = -450 \text{ mA};$	-	1.19	2.1	nC
Q_{GS}	gate-source charge	$V_{GS} = -4.5 V; T_j = 25 \text{ }^\circ C$	-	0.17	-	nC
Q_{GD}	gate-drain charge		-	0.1	-	nC
C_{iss}	input capacitance	$V_{DS} = -10 V; f = 1 \text{ MHz}; V_{GS} = 0 V;$	-	43	-	pF
C_{oss}	output capacitance	$T_j = 25 \text{ }^\circ C$	-	14	-	pF
C_{rss}	reverse transfer capacitance		-	8	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -10 V; I_D = -0.45 \text{ A}; R_L = 22 \text{ } \Omega;$	-	2.3	-	ns
t_r	rise time	$V_{GS} = -4.5 V; R_{G(ext)} = 6 \text{ } \Omega; T_j = 25 \text{ }^\circ C$	-	5	-	ns
$t_{d(off)}$	turn-off delay time		-	13.5	-	ns
t_f	fall time		-	6	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = -115 \text{ mA}; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-0.7	-1.2	V

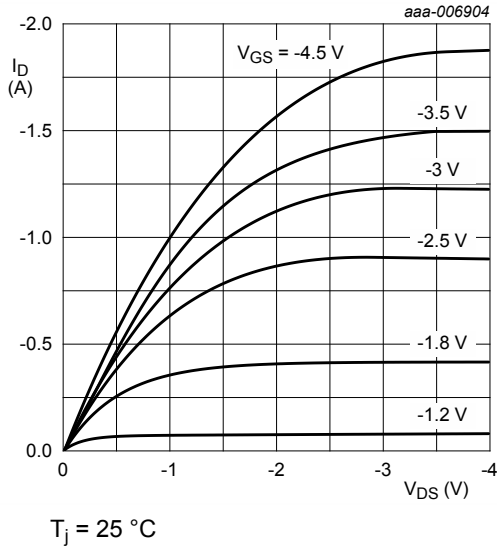


Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values

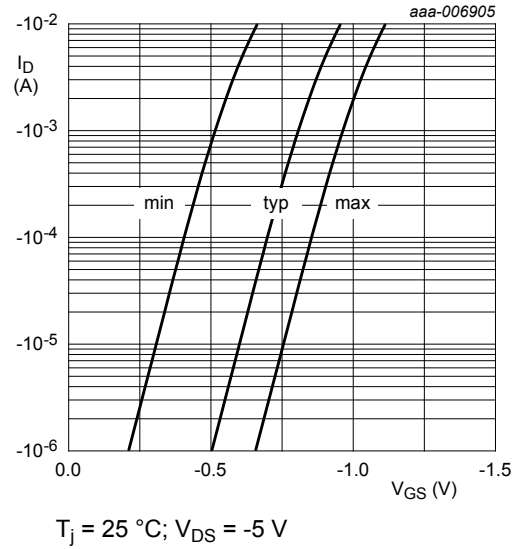


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

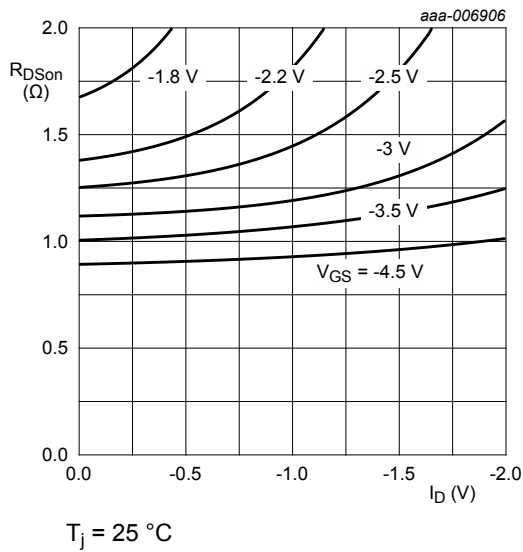


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

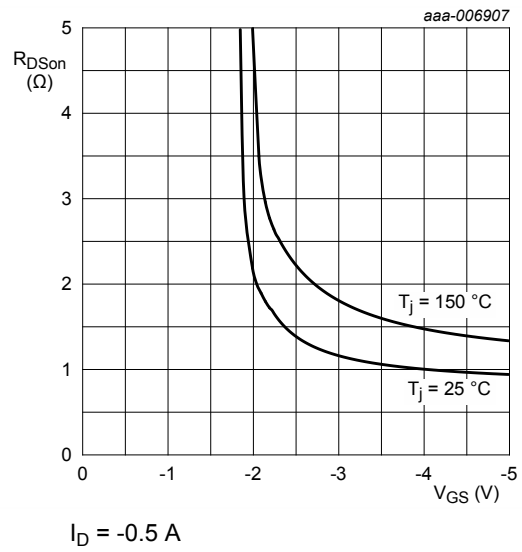
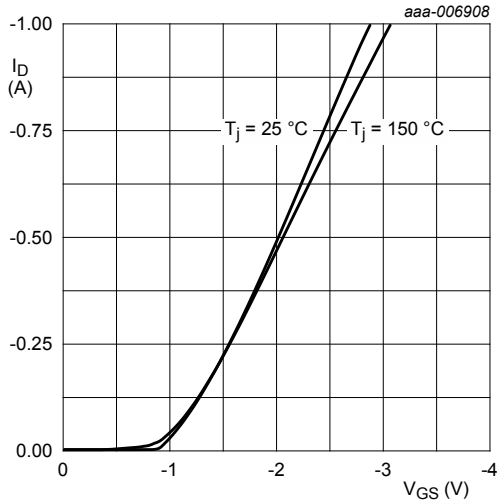


Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values



$$V_{DS} > I_D \times R_{DSon}$$

Fig. 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values

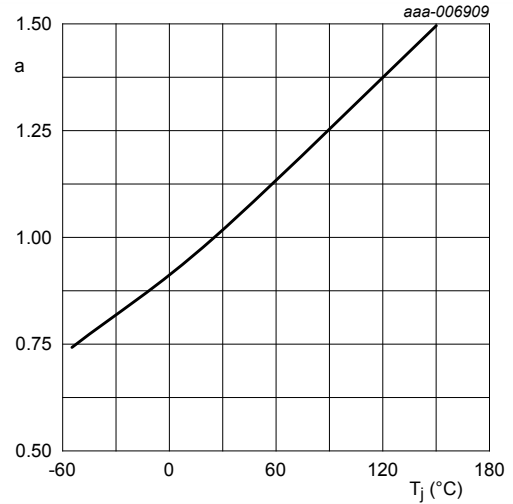
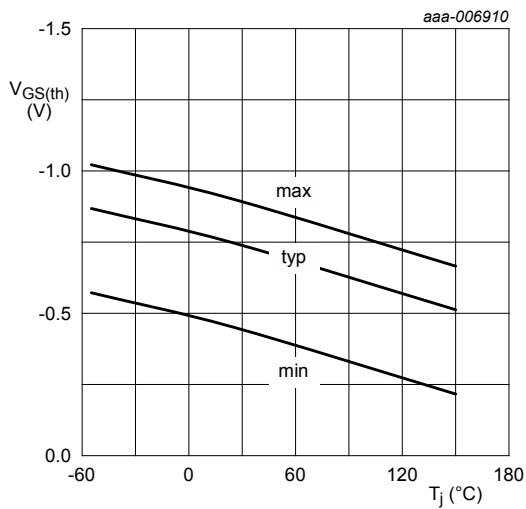


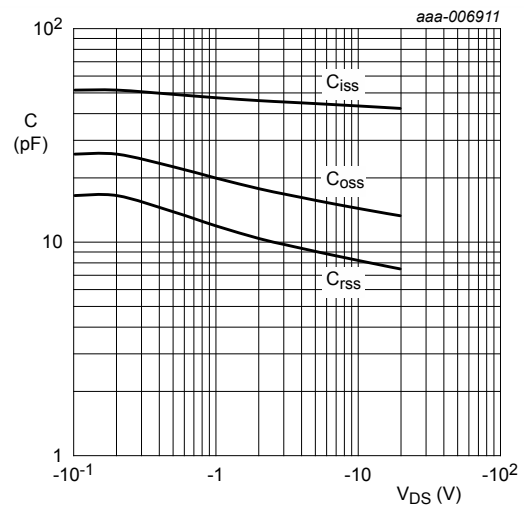
Fig. 12. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ C)}}$$



$$I_D = -0.25 \text{ mA}; V_{DS} = V_{GS}$$

Fig. 13. Gate-source threshold voltage as a function of junction temperature



$$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$$

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

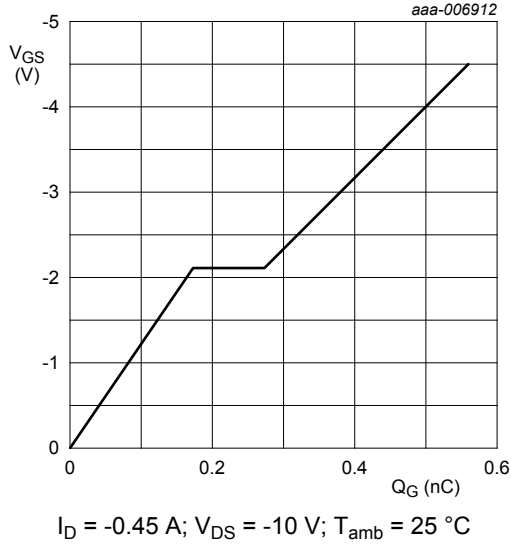


Fig. 15. Gate-source voltage as a function of gate charge; typical values

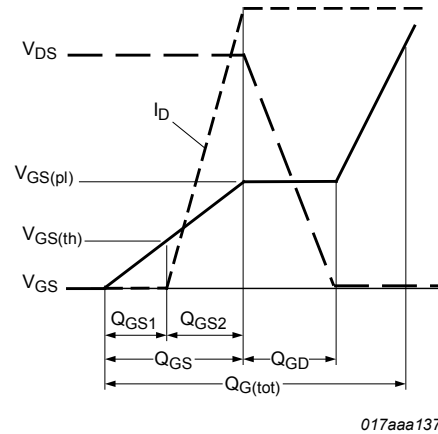
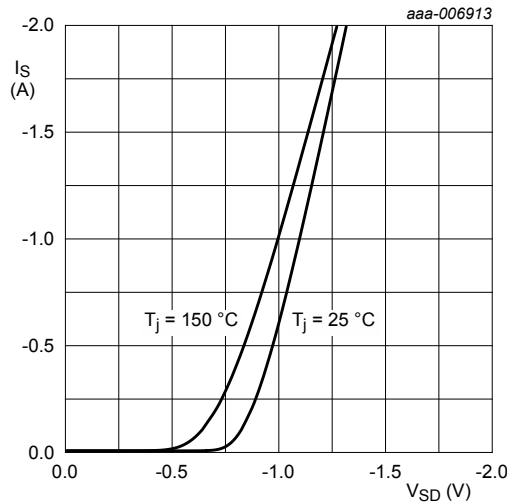


Fig. 16. MOSFET transistor: Gate charge waveform definitions



$V_{GS} = 0$ V

Fig. 17. Source current as a function of source-drain voltage; typical values

11. Test information

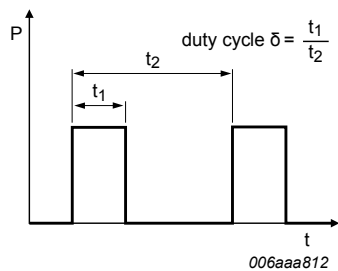


Fig. 18. Duty cycle definition

12. Package outline

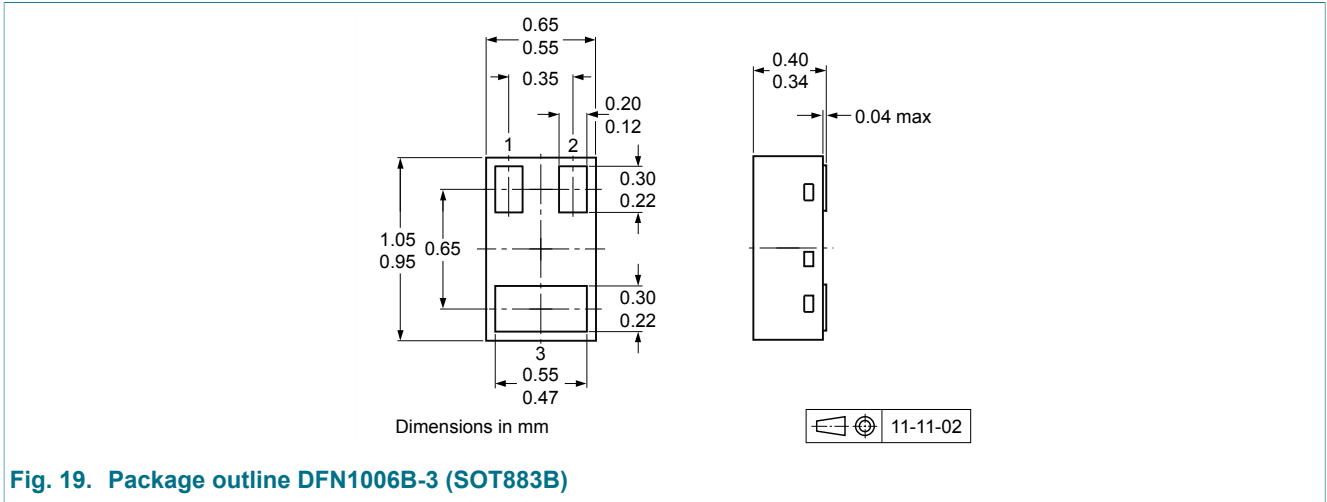


Fig. 19. Package outline DFN1006B-3 (SOT883B)

13. Soldering

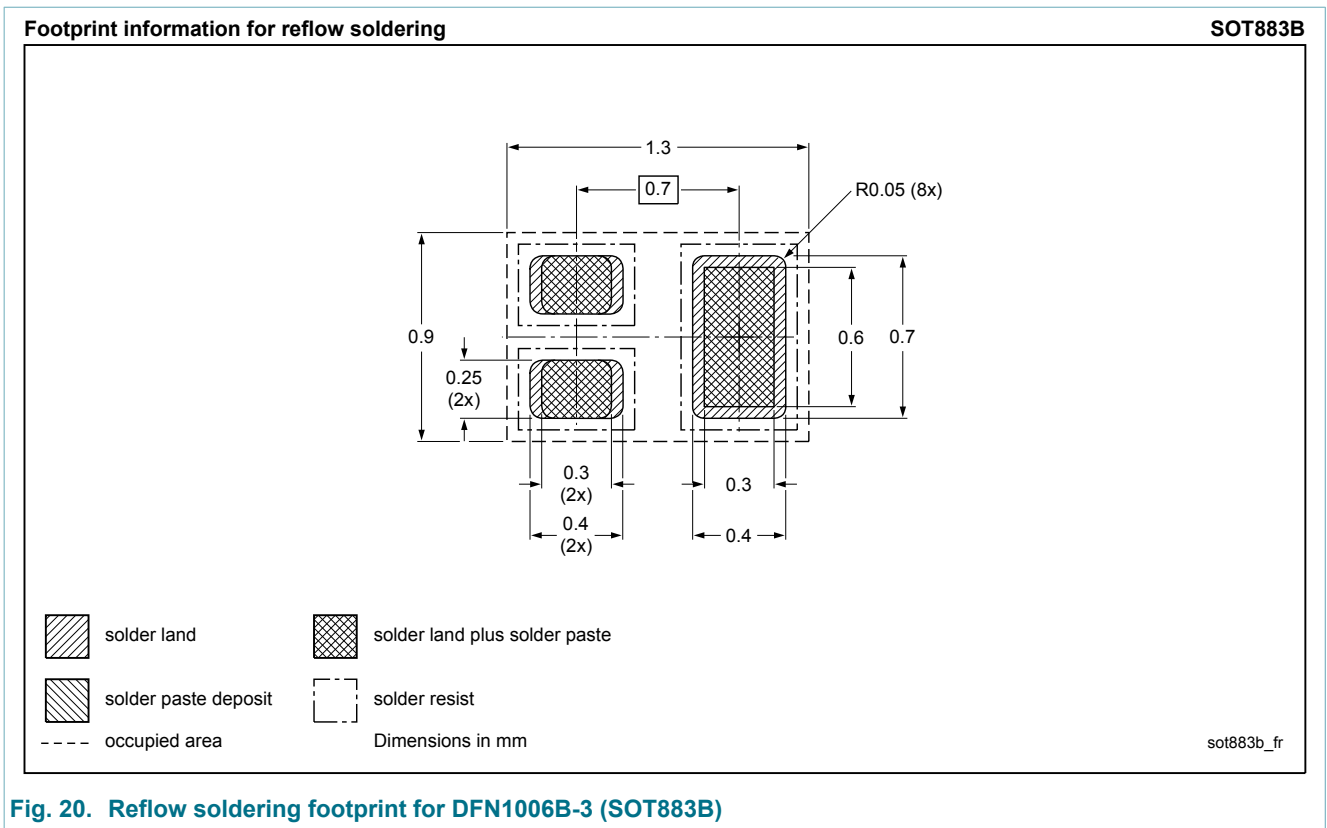


Fig. 20. Reflow soldering footprint for DFN1006B-3 (SOT883B)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMZB950UPE v.1	20140728	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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